

# Quantum-Safe Encryptor

## CHES CA5 Activities

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# AXE Group at Brno University of Technology



## **Applied Cryptography and Security Engineering (AXE):**

- based in Brno, Czech Republic,
- focused on PQC, PETs, Lightweight Crypto, SCA,
- delivering implementations for specific platforms: FPGA, smart-cards, constrained devices.

# Solutions to Quantum Threat

## Post-Quantum Cryptography

- easy integration with existing ICT, no special HW, cheap,
- existing SW implementations: OpenSSL 3.5, Open Quantum Safe,
- supported by national authorities: UK, US, Germany, France, Sweden, Netherlands, . . . ,
- FIPS standardization: CRYSTALS-Kyber, CRYSTALS-Dilithium, FALCON (lattice-based) and SPHINCS+ (hash-based)

**QKD - Quantum Key Distribution** - only key establishment.

**Hybrid Solutions** - combining PQC, classical cryptography, QKD.

# FPGA Quantum-Safe Encryptor I

- Demonstrator of FPGA Quantum-Safe Encryptor.



# FPGA Quantum-Safe Encryptor II

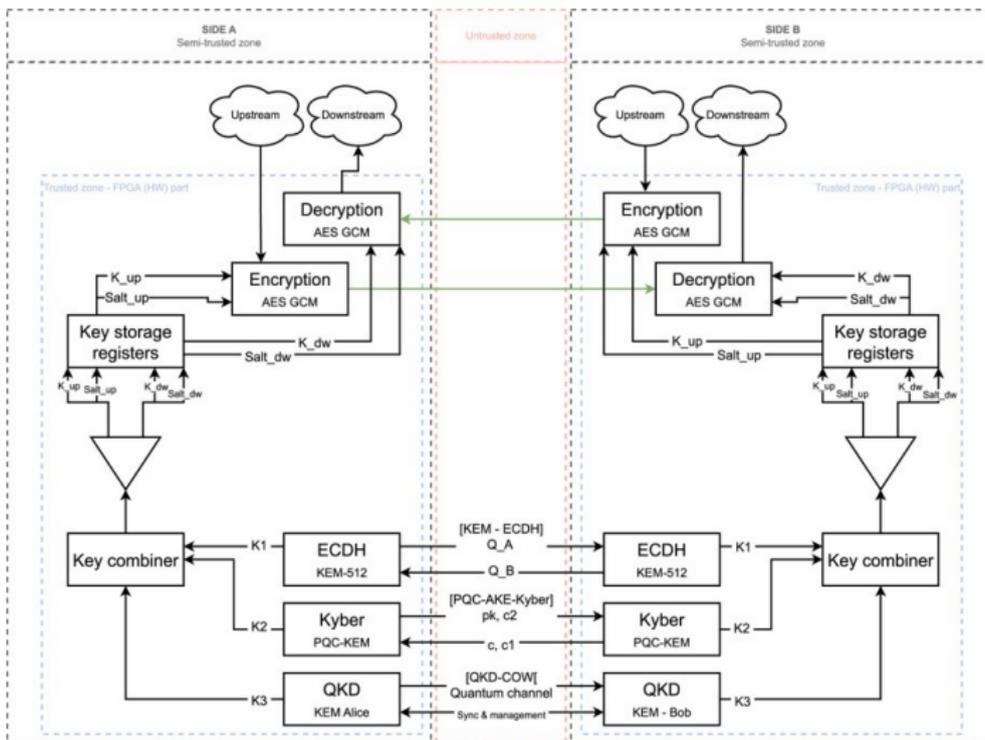
## FPGA Quantum-Safe Encryptor

- aim: hardware-accelerate high-speed encryptor for 100 GbE networks using standard TCP/IP protocols,
- hybrid KEM, keys from classical (ECDH), PQC (ML-KEM) and QKD (optional).
- implemented on programmable network interfaces with FPGA,
- supported by the Ministry of Interior (CZ), project NESPOQ #VJ01010008<sup>1</sup>, and tested/piloted by CHESSE.



<sup>1</sup><https://www.nespoq.cz>

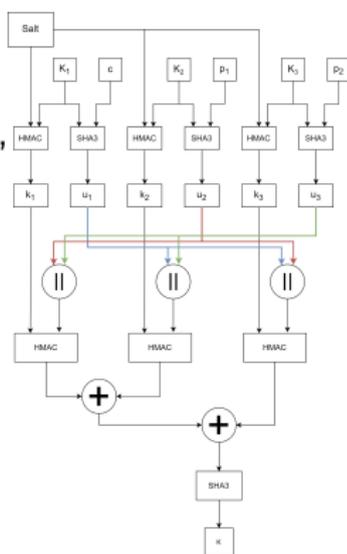
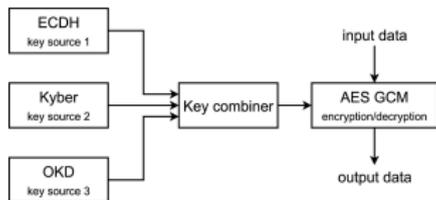
# FPGA Quantum-Safe Encryptor III



# FPGA Quantum-Safe Encryptor IV

## Cryptography components:

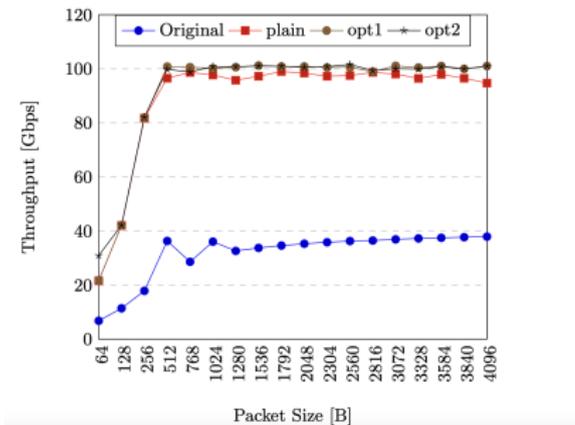
- Classical cryptography: ECDH-512,
- Quantum Key Distribution: IDQ Clavis 3,
- Post-Quantum: CRYSTALS-Kyber 768,
- Payload Encryption: AES-256-GCM,
- Key Combiner: own<sup>2</sup>.



<sup>2</sup>S. Ricci et Al, "Hybrid Keys in Practice: Combining Classical, Quantum and Post-Quantum Cryptography," in IEEE Access, vol. 12, 2024.

# FPGA Quantum-Safe Encryptor V

- Throughput: 117,3 Gbps<sup>3</sup>, high parallelism (for AES-GCM).
- Generating 1624 hybrid keys per second (without QKD).
- Monitoring via Grafana GUI.



<sup>3</sup>Cibik et al. Quantum-resistant hardware-accelerated IoT traffic encryptor, Internet of Things, 2025.

# FPGA Quantum-Safe Encryptor VI

## Optimization and Costs:

- originally designed for **Xilinx UltraScale+** FPGA chips,
- implemented and tested on **Silicom Denmark Mango** cards (approx. 10K EUR),
- and adapted for **Intel Agilex** (approx. 4K EUR),
- implemented and tested on **Intel N6010** (approx. 3K EUR),
- since 2025: **IP Cores commercially available**,
- currently: SCA resistance using masking techniques.



# Conclusion

- First hybrid encryptor (PQC ML-KEM, ECDH, QKD).
- Extreme performance: up to **100 Gbps**.
- Protected against side channel attacks.
- Piloted between Czechia and Estonia: BUT and CYBERNETICA.
- Supported by CHES CA5.



# Thank you for your attention.

Video: <https://www.youtube.com/watch?v=an5DwtZ1BjQ>



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